WHITE PAPER
Intel® Xeon® Processor 5500 Series
Storage

The New Intel® Xeon® Processor 5500 Series Catapults Processor Performance, Scalability, and Efficiency—A Huge Win for the Storage Industry.

"Intel microarchitecture provides a complete instruction spanning across multiple segment and power envelopes."

EXECUTIVE SUMMARY

The new regime of quad-core processors and platforms arrives with the Intel® Xeon® processor 5500 series, formerly code named Nehalem. As Intel continues its evolutionary tick-tock tempo to meet stringent requirements for better performance, cost, and data management competencies, the Intel microarchitecture brings together a comprehensive set of advanced technologies suited for the high-performance rigor of storage workloads not previously available in one set of blueprints.

The Intel Xeon processor 5500 series refines almost every facet of the microprocessor with substantial modifications to system architecture and memory structure. Several innovative developments include Intel® QuickPath Technology with integrated DDR3 memory controllers that replace the front-side bus; PCI Express 2.0* with twice the bandwidth per port of its predecessor; and Intel Hyper Threading Technology for increased resource utilization; and a shared L3 cache for better data movement capabilities.

The Intel Xeon processor 5500 series highlights the power of Intel microarchitecture with dynamic scalability and breakthrough performance, creating the foundation for a high I/O storage solution. The Intel Xeon processor 5500 series platform includes Intel Xeon processor 5500 series processors and the Intel® 5520 Chipset, providing the Intel Xeon-class reliability, availability, and serviceability features server storage platforms require. This paper provides several configuration options for the Intel Xeon processor 5500 series to meet various storage platform requirements.

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Overview: Intel Delivers Innovation Like Clockwork

Year after year, Intel delivers on its promise of reliable innovation using a "tick-tock" model for microprocessors, alternately releasing next-generation process technology and microarchitecture. Intel microarchitecture spans multiple segment and power envelopes with a common instruction set.

The tick is the shrinking of silicon process technology for the preceding microarchitecture, while every tock is the debut of a new microarchitecture. This metered rhythm enables Intel design teams to work in parallel for more efficient technology development and industry-leading product performance.

After the successful launch of the Intel® Xeon® processor 5400 family (the tick) with state-of-the-art 45nm high-k metal gate silicon technology, comes the next big tock, the introduction of Intel Xeon processor 5500 series, formerly code-named Nehalem.

The modern business environment cannot afford gluttonous inefficiencies in the data center. In particular, the storage community must address high levels of reliability, performance, availability, and scalability while supporting customer, vendor, and compliance requirements—usually all at once. So it is paramount that every operation, every system be as cost effective, energy efficient, and performance driven as possible.

The Intel Xeon processor 5500 series is expected to address these imperatives.

Improving Performance Every Leap of the Way

If performance is king, then speed, energy efficiency, and dynamic scalability are pillars of the castle. The Intel Xeon processor 5500 series provides the biggest architectural revamp to Intel's x86 processor line since the introduction of Intel® Pentium® Pro Processors in 1995. Intel microarchitecture offers the basic building blocks Intel will use to power all major computer platforms and support high-end servers and enterprise applications for years to come.

The Intel Xeon processor 5500 series employs many advanced concepts, extending the performance leadership of the Intel® Core™ microarchitecture and exploiting the energy efficiency and computing power of new 45nm high-k process technology. This new architecture provides multi-process multi-threaded performance with up to four cores per processor, Intel® Hyper-Threading Technology (Intel® HT Technology), and a shared last-level cache hierarchy. With the Intel Xeon processor 5500 series, the front-side bus gives way to integrated DDR3 memory controllers woven together with a high-speed, point-to-point interconnect known as Intel® QuickPath Technology at speeds up to 25.6 GB/sec bandwidth in this generation. The Intel Xeon processor 5500 series also applies the Intel SSE4.2 instruction set for enhanced string, text and XML processing.

Key Intel Microarchitecture Attributes of Storage-Worthy Note

The Intel Xeon processor 5500 series mixes a variety of features to meet the needs of many products and market segments. For the storage industry, that usually means scalable performance and adequate power envelopes to meet stringent enterprise-level requirements.

Key architectural attributes of the new Intel microarchitecture include:

- Intel QuickPath Technology with integrated DDR3 memory controller
- Integrated DDR3 memory controller for outstanding memory performance

- PCI Express 2.0* (PCIe 2.0*) for greater flexibility and bandwidth
- Shared L3 Cache Hierarchy for more efficient use of cache resources
- Hyper Threading for enabling a more energy efficient means of increasing performance for multi-threaded workloads
- Dynamic power/performance management for greater cost-efficiency thresholds
- Extending scalar performance with SSE4.2 Instruction Set Architecture (ISA) CRC32 for iSCSI

"Intel QuickPath Technology implements scalable shared memory by retiring the front-side bus method of accessing memory and I/O, and allowing each processor to have its own dedicated memory."

Intel® QuickPath Technology

Intel's new interconnect design is integral to achieving balanced and superior overall performance. The Intel QuickPath Technology integrates a DDR3 memory controller into each microprocessor and unites processors and other components, such as external memory or the I/O hub with a high-speed interconnect. Intel QuickPath Technology delivers the added performance and reliability, plus best-in-class bandwidth (up to 25.6 GB/sec) and low latency, to support future generations of dynamically scalable, multi-core processors, and platforms.

Intel QuickPath Technology implements scalable shared memory by retiring the front-side bus method of accessing memory and I/O, and allowing each processor to have its own dedicated memory. In this way, each processor can access its memory directly through an integrated memory controller. When a processor needs to access the dedicated memory of another processor, it does so through the Intel QuickPath Technology, which links all the processors in a point-to-point manner. Data is then sent in parallel across multiple lanes and processors no longer have to compete for front-side bus bandwidth, helping to increase I/O and memory performance of storage applications.

Intel QuickPath Technology also reduces the amount of communication needed for multi-processor systems to deliver faster payloads. Dense packet and lane structure usher up to roughly 5.87 billion data transfers per second, improving overall system performance. Intel QuickPath Technology takes advantage of tightly integrated reliability, availability, and serviceability (RAS) for highest processor resilience, as well as optional self-healing features, automated clock failover and rerouting, and hot-plug capabilities.

Integrated DDR3 Memory Controller

Intel uses an integrated ECC capable DDR3 memory controller for outstanding memory performance with up to 32 GB/sec memory bandwidth per integrated controller. The DDR3 is the latest synchronous dynamic random access memory (SDRAM) interface technology used for high bandwidth storage of a computer's working data. The key advantages of DDR3 are higher bandwidth—delivering twice the data transfer rate of DDR2 for much higher bus rates and higher peak rates—and increased performance with lower power requirements than DDR2.

PCI Express 2.0*

Intel QuickPath Technology takes advantage of PCIe 2.0 for greater flexibility and reliability in design and data transfer protocols. Delivering up to 16 GB/sec bandwidth per port—twice that of PCI Express 1.0*—PCIe 2.0 provides significant performance improvement for graphics-intensive applications such as sophisticated digital media and gaming. PCIe 2.0 devices communicate through the point-to-point interconnect to send and receive ordinary requests (i.e., configuration read/write, I/O read/write, memory read/write) and interrupts.

PCIe 2.0 allows storage applications to access more data faster and connect more devices than before—or gain twice the performance for the same number of connected devices. PCIe 2.0 enables scalable performance, high-bandwidth/low lane-count implementations, cost-effective silicon component designs, low overhead/low latency data transfers, and backwards compatibility with PCI Express 1.0.

Shared L3 Cache Hierarchy

The Intel Xeon processor 5500 series enhances the Intel® Smart Cache technology of previous processors by adding an inclusive, shared last-level cache (LLC), meaning the cache can be shared across all cores. The new cache hierarchy is designed to improve performance of multi-thread applications by making it easier to share data and more efficiently utilize cache resources.

Architectures that use exclusive LLC cache contain data not stored in other caches. If a data request misses on this LLC cache, all cores would need to be searched or "snooped" to locate the missing data, adding latency and reducing performance. By adding a shared or inclusive last-level cache, Intel Xeon processor 5500 series guarantees that the data is outside the processor, helping to eliminate unnecessary snoop traffic and improve performance. Intel Xeon processor 5500 series' inclusive LLC cache can be configured up to 8 MB in size, and all applications can use the entire cache.

A new two-level Translation Lookaside Buffer (TLB) system is also included with the Intel Xeon processor 5500 series. A TLB is a processor cache that is used by memory management hardware to improve the speed of virtual to physical address translation. While all current desktop and server processors use a TLB, the Intel Xeon processor 5500 series adds a new second level 512 entry TLB to further improve performance.

Intel® Hyper-Threading Technology

Most multi-core processors enable executions of one thread per processor core, but the Intel Xeon processor 5500 series bends the rules to enable Intel® HT Technology within each processor core, doubling the number of threads that can be concurrently processed at the same time. Intel HT Technology permits more efficient workloads and processing muscle than just adding more cores. Consequently, storage servers can virtualize more applications, digital media can power up faster, and high-end computing models can process tasks quicker. Because Intel HT Technology is more energy efficient than traditional threading workloads, Intel Xeon processor 5500 series-based products can operate eight simultaneous threads per quad-core processor and 16 simultaneous threads for dual-processor quad-core designs.

Dynamic Power/ Performance Management

Because energy efficiency across the IT enterprise is essential to trimming costs and optimizing resources, the microarchitecture must address power constraints while still delivering processor performance. Intel Xeon processor 5500 series includes a strict power/performance efficiency threshold.

When determining the new microarchitecture, Intel carefully scrutinized each architectural feature. If a feature could not add more than a one percent performance gain versus one percent power gain for a less than three percent power cost, Intel did not include it. By measuring performance gains against power costs, Intel was able to design the next-generation microarchitecture to deliver greater power efficiency at any power envelope. Intel Xeon processor 5500 series blueprints the proper performance/power requirements to carry out intense payloads and high-performance computing without the power drain.

Built on Intel® Microarchitecture: The Intel Xeon Processor 5500 Series

IDC predicts that by the year 2015, the IT industry will embrace 15 billion intelligent, connected devices.[1] Getting those results means finding inventive ways to support both old and new technologies, lower latencies, greater throughputs and capacities—without sacrificing performance or power efficiencies.

The Intel Xeon processor 5500 series helps facilitate faster, smarter devices for breakthrough performance, reliability, and enterprise server compatibility, the new Intel microarchitecture consists of the Intel Xeon processor 5500 series, the Intel 5520 chipset and the ICH10R I/O Controller Hub. There are four processors in the family offering the long life support that storage platforms typically require:

- Intel® Xeon® Processor E5540 with Standard Thermals
- Intel® Xeon® Processor E5504 with Standard Thermals
- Intel® Xeon® Processor L5518 with Robust Thermals
- Intel® Xeon® Processor L5508 with Robust Thermals

Ideal as a high I/O storage platform, the Intel Xeon processor 5500 series supports dual-processor configurations and even dual IOH architectures—offering up to 72 lanes of PCIe 2.0 connectivity—to help meet rigorous bandwidth requirements of today's Serial Attached (SAS), Fibre Channel, Fibre Channel over Ethernet, and 10 Gb Ethernet.

Configuration Options

The Intel Xeon processor 5500 series supports multiple platform configuration options, each intended for maximum versatility and flexible connectivity choices. The PCIe Non-Transparent Bridge (NTB) feature displayed in each configuration is representative of a third-party device offering that provides system memory isolation and a "doorbell" mechanism to deliver messages between canisters.

Single CPU, Single IOH

The usage example shown in Figure 1 includes one Intel® 5520 I/O Hub to provide a smaller footprint single-socket design for dense, high-performance, and redundant storage controllers. This configuration is ideal for achieving balanced processor and I/O storage workloads, delivering fast DDR3 memory interfaces for high I/O data paths, and meeting higher ambient temperatures in Storage Bridge Bay (SBB) canisters with Intel's high Tcase processors.

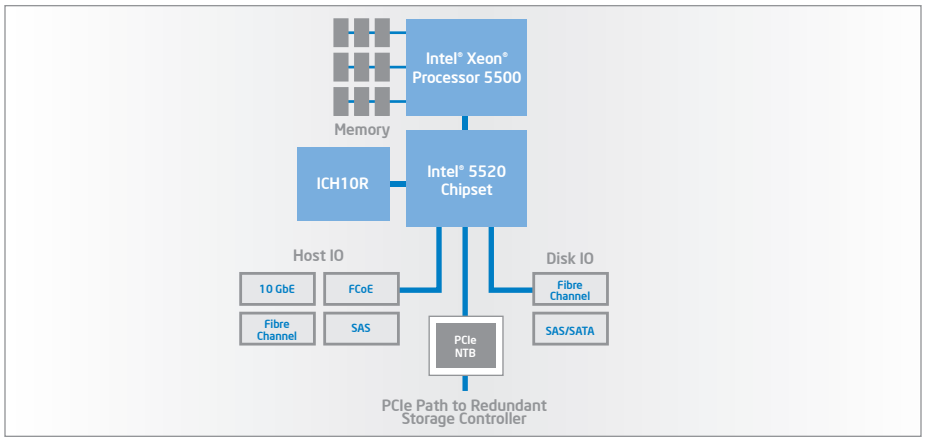

Figure 1. Single processor, single IOH.

Dual Processors, Single IOH

This usage example depicts a high-performance storage platform (see Figure 2.) The architecture is designed for strong processor and memory controller performance with high-performance, flexible PCIe 2.0, and is ideal for converged storage and server platforms, and managing high-performance RAID and storage workloads.

The dual processor, single IOH model includes large capacity DDR3 for storage caching, up to 36 lanes of PCIe 2.0 connectivity, and support for leading technology interfaces such as 6 Gb/s SAS, Fibre Channel, FCoE, and 10 GbE.

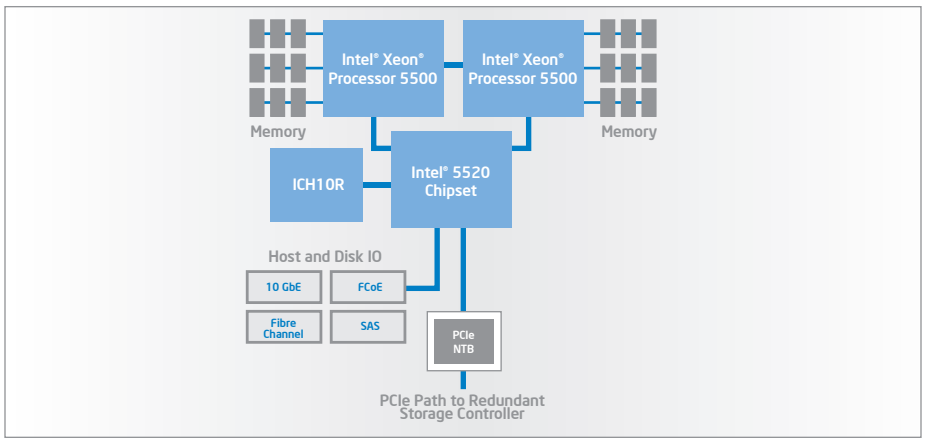

Figure 2. Dual processors, single IOH.

Dual Processors, Dual IOH

In this usage example, there are dual processors and dual I/O hubs used for a high I/O connectivity storage platform (see Figure 3.) The dual IOH architecture is designed for platforms requiring high lane count PCIe 2.0 support.

The dual IOH option doubles the number of lanes available for PCIe 2.0 connectivity to 72, and meets requirements for multiple, high-bandwidth SAS, Fibre Channel, FCoE, and 10 GbE interfaces.

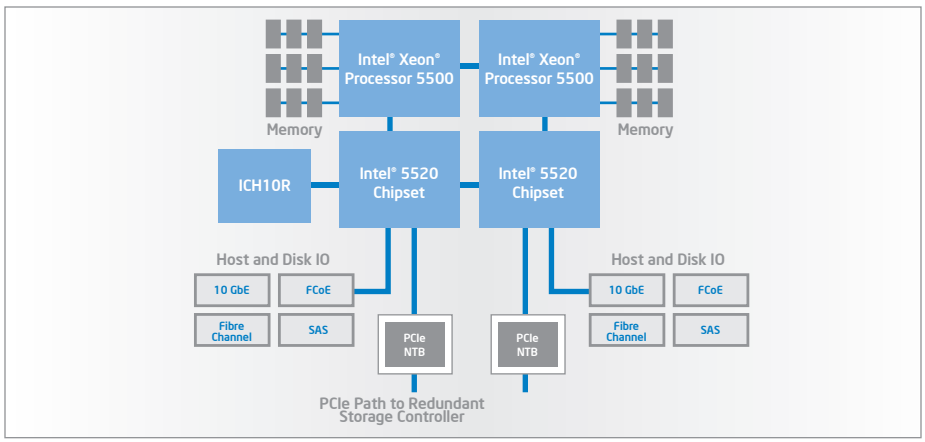

Figure 3. Dual processors, dual IOH.

Gaining a New Level of Storage Benefits

With the Intel Xeon processor 5500 series come positive effects for storage platform design. As with any storage platform, the key is to move data from disk to network and back as fast and safely as possible. Platforms built on Intel michroachitecture, such as the Intel Xeon processor 5500 series, offer sweeping technical leaps required to exceed expectations for moving that data.

"From the Intel Xeon processor 5500 series, customers are able to gain a flexible, scalable platform architecture for enterprise storage."

Products built on the features of Intel Xeon processor 5500 series will be well positioned to achieve balanced integration and performance, while facilitating dynamic scalability. Some vendors design "bare metal" storage-specific processors that require storage design expertise to assemble the right mix of components and calculations for building a platform. Intel applies a holistic design approach that comprises best-in-class components (processors, bus, I/O) which are intended to work together. As a result, Intel processors and platforms enable high performance, power efficiency, and dynamic scalability that are ideal for supporting enterprise storage applications.

Other vendors sometimes reuse standard server designs for enterprise storage. For example, from one Intel platform, storage engineers can create many derivative products for different levels of performance or scalability—simply by changing the processor or the number of cores. By staying within one Intel platform, customers can scale up or down for a fraction of the investment of creating a whole new storage platform based on assembled parts.

Conclusion

The Intel Xeon processor 5500 series is Intel's next-generation design triumph, complete with a suite of features aimed at extending the performance leadership of previous Intel microarchitecture and the new 45nm high-k metal gate silicon technology. Designed for dynamic modular scalability, outstanding performance, and highly efficient power thresholds, the Intel Xeon processor 5500 series includes advanced technologies such as Intel QuickPath Technology with integrated DDR2 memory controllers, PCIe 2.0, shared L3 cache, and SMT.

Mainstream processors and platforms built on the Intel Xeon processor 5500 series will be primed to provide robust performance and power efficiency for even the most demanding enterprise storage applications.

For more on Intel Xeon processor 5500 series, see:
www.intel.com/p/en_US/products/server/processor/xeon5000

[1] Source: John Gantz, IDC CRO.

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